REMARKS

Claims 1, 2, and 4-20 are presently pending. Claims 11-16 are withdrawn from consideration pursuant to an earlier restriction requirement. Claims 1, 2, 4, 10, 17, and 20 have been rejected. Claims 5-9, 18 and 19 have been objected to as being dependent upon a rejected base claim, but indicated allowable if rewritten in independent form. Applicants appreciate Examiner's indication of allowable subject matter. No claims have been amended.

Independent claims 1 and 2 were rejected under 35 U.S.C. 102(e) as anticipated by Lee, and under 35 U.S.C. 103(a) as obvious from Jeddeloh in view of Lee. Claim 17 was rejected under 35 U.S.C. 103(a) as obvious from Lee. Reconsideration in view of the following remarks is respectfully requested.

IN LEE, THE LOGIC DOES NOT RECEIVE SIGNAL DSQW FROM RESPONDING NODE 43

Examiner has stated that Lee discloses "logic (Fig. 7-8) for transmitting a signal DQS to the requesting node indicating presence of the response if the logic receives a signal DSQW from the responding node 43 indicating the presence of the data within a predetermined period of time (VDQSWIN1-2, Fig. 5-6) after receiving the signal from the request node indicating the presence of the request." Office Action, pp. 2-3 (Emphasis Added).

Applicants respectfully traverse because in Lee, the logic (Fig. 7-8) does not "receive a signal DSQW from the responding node 43". Applicants first call Examiner's attention to Lee, Figure 7. "FIG. 7 is a circuit for writing data in to a DDR synchronous DRAM". Lee, Col. 4,

Lines 17-18. In Lee, Figure 7, there is no indication that the signal DQSW is received from the responding node 43. Moreover, the "indication signal DQSW … is preferably generated by the memory controller 41, during a write operation". Lee, Col. 4, Lines 64-65. Applicants next call Examiner's attention to Lee, Figure 8. In FIGURE 8, the signal DQSW is transmitted by the circuit shown therein.

Accordingly, Applicants respectfully submit that Lee does not teach or fairly suggest the claimed "logic for transmitting a signal to the requesting node indicating the presence of the response if the logic receives a signal from the responding node indicating the presence of data within a predetermined period of time after receiving a signal from the requesting node indicating the presence of the request." Examiner is requested to withdraw the rejection under 35 U.S.C. 102(e) to claims 1, 2, 4, and 10, as well as the rejection under 35 U.S.C. 103(a) to claims 17, and 20.

PREDETERMINED PERIOD OF TIME AFTER RECEIVING SIGNAL

Applicants additionally note that, even assuming *arguendo* that in Lee the "logic receives a signal DQSW from the responding node" (which for the reasons described above, it does not), Lee does not teach that "logic for transmitting a signal DQS to the requesting node indicating presence of the response if the logic receives a signal DSQW from the responding node 43 indicating the presence of the data within a predetermined period of time (VDSQWIN1-2, Fig. 5-6) after receiving the signal from the requesting node indicating the presence of the request" as claimed by Examiner. Office Action at 2-3. (Emphasis Added).

Examiner has not explicitly identified where in Lee there is logic "receiving the[1] signal from the requesting node indicating the presence of the request", however, Examiner has indicated a "requesting node (memory controller 41) for transmitting a request (COM, read/write request)". Id. Applicants call Examiner's attention to Lee, Figures 5 and 6, where VDQSWIN1 and VDQSWIN2 are indicated to begin at the falling edge of DQSW. Applicants respectfully submit that there is no indication that "transmission of DQS to the requesting node" is based on the condition "if the logic receives a signal DSQW ... within a predetermined period of time after receiving a signal from the request node...".

JEDDOLEH IN VIEW OF LEE

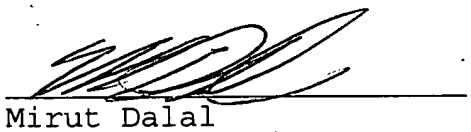
Examiner notes that "Jeddeloh does not specifically disclose that the indicating signal is within a predetermined time interval" and Examiner does not allege that Jeddeloh teaches "a predetermined period of time after receiving a signal from the request node". For the above reasons, Lee also does not teach or fairly suggest "logic for transmitting a signal to the requesting node indicating the presence of the response, if the logic receives a signal from the responding node indicating the presence of data within a predetermined period of time after receiving a signal from the requesting node indicating the presence of the request." Accordingly, the combination of Jeddeloh and Lee does not teach or fairly suggest the foregoing limitation. Applicants request Examiner withdraw rejections to claims 1, 2, and 4 under 35 U.S.C. 103(a).

[1] Claims 1, 2, and 17 claim "receives/receiving a signal" (Emphasis Added).

CONCLUSION

For the foregoing reasons, independent claims 1, 2, and 17 are allowable, as well as dependent claims 4-10, and 18-20 are allowable. Therefore, each of the pending claims are allowable, and Examiner is hereby requested to pass this case to issuance.

Respectfully submitted,



Date:

Mirut Dalal
ATTORNEY FOR APPLICANTS
Reg. No. 44,052

McANDREWS, HELD & MALLOY, LTD.
500 West Madison - Suite 3400
Chicago IL 60661

PHONE (312) 775-8000
FAX (312) 775-8100